Amendments to the Specification:

Please replace the paragraph (or section) beginning at page 8, line 19, with the following redlined paragraph (or section):

After a predetermined time delay, the t-req signal to the target is asserted. ~~This is when the contents of the FIFO, that is the FIFO depth, reaches the programmed or preset limit. Alternatively, the~~ The time delay could be a predetermined number of clock cycles of either buffer input or output clock. If the target is able to receive data it returns a t-gnt signal. With both t-req and t-gnt equal to 1, data is now clocked out of the transmit FIFO. A t-req will also be generated if an end of packet signal is received, that is I-eop = 1, indicating that this word is the last in a packet. Once the t-req signal is asserted, whether because the limit is reached or because an end of packet indicator is received, it is de-asserted or returned to zero only when the transmit FIFO becomes empty, all data having been clocked out of it.